Global IP Core Sales®

DVB-S2 Demodulator

DVBS2_DEMOD.vhd performs the demodulation based on three tracking loops: carrier tracking (for coherent demodulation), symbol timing tracking, and AGC. Each output bit's quality is expressed as Log-Likelihood Ratio (LLR) for use. The receiver operates in two clock domains: global clock CLKRXg (half the ADC sampling rate) is mostly for demodulation.

Key Features and Performance:

- Flexible programmable features:
- Modulation symbol rate, frequency offset, SRRC filter roll-off.
- Output type: BBFRAME or stream (transport stream, generic stream packetized, generic bit stream)

Supported Features:

- Inputs: two DDR complex (I,Q) baseband samples, 16-bit precision. ADC sampling rate is twice the clock frequency fCLK RXg
- Maximum payload bit rate: > 675 Mbits/s (8-PSK, rate 9/10, Xilinx Ultrascale+ -2)
- Modulation type: Automatic detection on a frame-to-frame basis: QPSK, 8-PSK, 16APSK, 32APSK
- Maximum modulation symbol rate (ultrascale+ -2 speed grade): > 250 MS/s
- Output: -Single or multiple MPEG Transport Stream. 188-Byte fixed length frames, Bytewide.
  -Single or multiple Generic Stream (packetized or continuous). Byte-wide.

IP Core Deliverables:

- VHDL source code
- GNU radio project and Matlab conversion .m program for generating DVB-S2 waveforms.
- VHDL testbench
- PRBS11 test sequence generator, AWGN noise generator

A comprehensive DVB-S2 Demodulator datasheet can be provided under an NDA, please contact info@global-ipc.com.

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