

## The NavIC BCH Decoder FEC IP Core

The NAVIC BCH Decoder FEC IP Core is developed for satellite navigation applications.

### **Benefits**

- Low Area Design
- Low-power and low-complexity design
- Maximum likelihood decoder
- Soft-decision decoding

### **Features**

- Compliant with 'ISRO-NAVIC-ICD-SPS-L1-1.0' standard [1]
- Supports the BCH decoding for subframes (TOI) signal

### **Key Features**

- Throughput matching the required specifications
- Bit-error-rate (BER) and block-error-rate (BLER) performance meet the required specifications

### **Deliverables**

- Synthesizable Verilog
- System Model (Matlab)
- Verilog Testbenches
- Documentation

### **Applications**

- Satellite Navigation
- Global Positioning Service receiver

Please contact us for more information at [info@global-ipc.com](mailto:info@global-ipc.com) or check out our product portfolio at [www.global-ipc.com](http://www.global-ipc.com)

### **About Global IP Core Sales**

Global IP Core Sales® was founded in 2021 and provides state-of-the-art IP Cores for the Semiconductor market. The majority of our products are silicon proven and can be seamlessly implemented into FPGA and ASIC technologies. Global IP Core Sales® will assist you with your IP Core and integration needs. Our mission is to grow your bottom line.

*A comprehensive NavIC BCH Decoder FEC IP Core datasheet can be provided under an NDA, please contact us at [info@global-ipc.com](mailto:info@global-ipc.com).*