

Flash Memory LDPC Decoder IP Core Available For Integration From Global IP Core

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messages are sent from the check nodes to bit nodes after the SPA steps which are (for one iteration): initialization of all bit nodes by the Log-likelihood ratios (LLRs) from the channel; for all check nodes and in the bit nodes positions corresponding to 1 in the H matrix, calculation of the variable nodes updates are

done based on Log-tanh equation; for each variable node the total update is calculated by the summation of all updates that come from all check nodes which are connected to this variable node; at the end, the new variable nodes values are overwritten by adding the old variable nodes values to their corresponding total updates.

Min Sum Algorithm (MSA) is a simplified version of SPA where the calculation of the variable nodes updates per check equation are done based on finding the minimum value of the variable nodes absolute values and the product of their signs instead of Log-tanh equation.

The design of Flash Memory LDPC decoder is supplied as a portable and synthesizable Verilog IP.

Features Include:

- Quasi cyclic (QC) – Algebraic constructed – LDPC Code
- Regular Parity Check Matrix
- Codeword length: 16 K
- Code rate 0.953
- No or very low error floor
- Parallel/Layered decoding
- Soft decision decoding
- Configurable number of iterations

Deliverables:

- Synthesizable Verilog
- System Model (Mat Lab) and documentation
- Verilog Test Benches
- Documentation

Please contact us for more information at info@global-ipc.com or check out our product portfolio at www.global-ipc.com

About Global IP Core Sales:

Global IP Core Sales® was founded in 2021 and provides state-of-the-art IP Cores for the Semiconductor market. The majority of our products are silicon proven and can be seamlessly implemented into FPGA and ASIC technologies. Global IP Core Sales® will assist you with your IP Core and integration needs. Our mission is to grow your bottom line.