Global IP Core Sales®

Reed Solomon Encoder and Decoder

Overview

The Reed Solomon Encoder is fed with an input message of K information symbols, the Encoder appends 2T parity symbols to the input message in order to form the encoded codeword. The Reed Solomon Decoder receives an (N=K+2T) codeword, and it can locate and correct up to 8 possible symbol errors or up to 14 erasures. Both of the Encoder and the Decoder support any input timing pattern, in case of the Encoder; the output timing pattern will be the same as the input. In case of the Decoder; the output timing pattern is fully controlled in order to support any desired pattern by the user. The Reed Solomon Decoder keeps track of corrected errors. Input codewords with more than 8 errors are regarded as uncorrectable, and are flagged. The Implementation of Reed Solomon IP Core targets very low latency, high speed, and low gate count with a simple interface for easy integration on SoC applications.

Features

- High performance Reed Solomon IP Core (Encoder and Decoder)
- Supports error and erasure decoding
- Parameterized codeword length
- Code generator polynomial: $(x + \lambda^0)(x + \lambda^1)(x + \lambda^2) \ldots (x + \lambda^{15})$
- Field generator polynomial: $x^8 + x^4 + x^3 + x^2 + 1$
- The core supports any input or output timing pattern

Applications

- (Digital Video Broadcasting) DVB
- Digital Transmission of Television Signals (ITUTJ.83)
- WiMAX (IEEE Std 802.16d)

Deliverables

- Synthesizable Verilog
- System Model (Matlab)
- Verilog Test Benches
- Documentation
- FPGA testing environment

A comprehensive Reed Solomon Encoder and Decoder datasheet can be provided under an NDA, please contact info@global-ipc.com.

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