Global IP Core Sales®

DVB-S2 LDPC/ BCH Decoder and Encoder

The DVB-S2 LDPC-BCH block is a powerful FEC (Forward Error Correction) subsystem for Digital Video Broadcasting via Satellite. In Digital video broadcasting for digital transmission for satellite applications, a powerful FEC sub-system is needed. FEC is based on LDPC (Low-Density Parity Check) codes concatenated with BCH (Bose Chaudhuri Hocquenghem) codes, allowing Quasi Error Free operation close to the Shannon limit.

Features

- Irregular parity check matrix
- Layered Decoding
- Minimum sum algorithm
- Soft decision decoding
- BCH decoder works on GF (2m) where m=16 or 14 and corrects up to t errors, where t = 8, 10 or 12
- ETSI EN 302 307-1 V1.4.1 (2014-11) compliant

Key Features

- Long and short frame lengths
- No error floor to QEF in Standard
- Easy to integrate within receiver
- All code rates and modulation orders
- **Wideband support**

Benefits

- Improved performance
- Improved efficiency wrt Shannon's limit
- Very high data rate

Applications

- DVB-S2

Deliverables

- Synthesizable Verilog
- System Model (Matlab)
- Verilog Test Benches
- Documentation

A comprehensive DVB-S2 LDPC/ BCH decoder and encoder datasheet can be provided under an NDA, please contact info@global-ipc.com.

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