Global IP Core Sales®

DVB-RCS2 Turbo Encoder & Decoder

Features

- 16-state double binary turbo Encoder/Decoder
- Puncturing/De-puncturing on the fly
- Run time selectable number of iterations
- Parallel decoding algorithm
- Hard decision output
- Tail-bitten termination
- Fully compliant with DVB-RCS2 code rates
- Supports MAX-log-MAP Algorithm
- Sliding window algorithm for internal memory reduction.
- Uses parallel internal interleaver/de-interleaver

System Overview

On the transmitter side, the turbo-phi encoder architecture is based on a parallel concatenation of two double-binary Recursive Systematic Convolutional (RSC) encoders, fed by blocks of K bits (N=K/2). It is a 16-state double-binary turbo encoder.

On the receiver side, the turbo decoder engine is built using two functioning soft-in/soft-out modules (SISO). The outputs of one SISO, after applying the scaling and interleaving are used by its dual SISO in the next half iteration.

Both the turbo encoder and decoder are fully compliant with the DVB-RCS2, supporting all its code rates and block sizes.

Functional Description

In order to achieve higher throughput, the turbo decoder uses parallel MAP decoders. The sliding window algorithm is used to reduce the internal memory sizes. Turbo decoder accepts input LLR's and outputs the hard decision bits after completing the decoder iterations.

Deliverables

- Synthesizable Verilog
- System Model (Matlab)
- Verilog Test Benches
- Documentation

A comprehensive DVB-RCS2 Turbo encoder and decoder datasheet can be provided under an NDA, please contact info@global-ipc.com.

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