

DVB-RCS2 Turbo Decoder and Encoder IP Core Available For Integration From Global IP Core

February 6, 2023 - Global IP Core Sales - The new DVB-RCS2 Turbo Encoder and Decoder IP Core is on



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the transmitter side, the turbo-phi encoder architecture is based on a parallel concatenation of two double-binary Recursive Systematic Convolutional (RSC) encoders, fed by blocks of K bits ($N=K/2$). It is a 16-state double-binary turbo encoder. On the receiver side, the turbo decoder engine is built using two functioning soft-in/soft-out modules (SISO). The outputs of one SISO, after applying the scaling and interleaving are used by its dual SISO in the next half iteration. Both the turbo encoder and decoder are fully compliant with the DVB-RCS2, supporting all its code rates and block sizes.

Additional features include:

- 16-state double binary turbo Decoder/ Encoder
- Puncturing/De-puncturing on the fly
- Run time selectable number of iterations
- Parallel decoding algorithm
- Hard decision output
- Tail-bitten termination
- Fully compliant with DVB-RCS2 code rates
- Supports MAX-log-MAP Algorithm
- Sliding window algorithm for internal memory reduction
- Uses parallel internal interleaver/de-interleaver

Benefits:

In order to achieve higher throughput, the turbo decoder uses parallel MAP decoders. The sliding window algorithm is used to reduce the internal memory sizes. Turbo decoder accepts input LLR's and outputs the hard decision bits after completing the decoder iterations.

Related IP Core Products:

- DVB-RCS2

Please contact us for more information at info@global-ipc.com or check out our product portfolio at www.global-ipc.com

About Global IP Core Sales:

Global IP Core Sales® was founded in 2021 and provides state-of-the-art IP Cores for the Semiconductor market. The majority of our products are silicon proven and can be seamlessly implemented into FPGA and ASIC technologies. Global IP Core Sales® will assist you with your IP Core and integration needs. Our mission is to grow your bottom line.