

## CCSDS AR4JA LDPC Encoder and Decoder FEC IP Core Available For Licensing and Implementation from Global IP Core

**January 9, 2023 - Global IP Core Sales** - The new CCSDS AR4JA LDPC Encoder and Decoder FEC IP Core is



a configurable design that allows runtime configuration for decoding different code rates (i.e., 1/2, 2/3 and 3/4). To obtain high throughput, two different levels of parallelism are carried out; 128 check nodes and 6 variable nodes which are processed at the same time. Pipeline architecture is followed which significantly

speeds up the whole decoding process. Also, layered architecture is implemented which helps to enhance the speed of the decoding process. AR4JA LDPC decoder supports soft decision decoding and hard decision output.

### **Additional features include:**

- CCSDS AR4JA LDPC Code family is quasi-cyclic
- Irregular parity check matrix
- Run time configuration for more than one code rate (i.e., 1/2, 2/3, 3/4)
- Configurable codeword size that supports 2K, 3K, and 4K information words
- Minimum sum algorithm
- Layered decoding architecture
- Soft decision decoding

### **Benefits:**

- AR4JA LDPC code is characterized by faster convergence of bit-error rate (BER) with less number of iterations compared to quasi-cyclic codes. • Frame-to-frame on-the-fly configuration.
- The implemented design supports code rates 1/2 (N=8192, K=4096), 2/3 (N=3072, K=2048) and code rate 3/4(N=4096, K=3072).
- A trade-off exists among the design key parameters which are: code rate, decoding latency, power efficiency, throughput, and area.

### **Related IP Core (FEC) Products:**

- CCSDS
- FLASH Memory

Please contact us for more information at [info@global-ipc.com](mailto:info@global-ipc.com) or check out our product portfolio at [www.global-ipc.com](http://www.global-ipc.com)

### **About Global IP Core Sales:**

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